PATENT

Appl. No. 09/988,896
Amdt. dated November 11, 2005
Reply to Office Action of August 11, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended) A method of de-skewing data in a data communication system having a first chip for communicating a plurality of data-bits to a second chip through a data-bus, the method comprising:

forwarding a sequence of training bits from the first chip to the second chip;

receiving the sequence of training bits at the second chip;

comparing the sequence of training bits received to the sequence forwarded in order to determine if one training bit has a data skew;

if the training bit is not skewed, selecting a first input ~~(the no-skew input)~~ for receiving the plurality of data-bits;

if the training bit is skewed, determining whether there is a late skew or an early skew;

if a late skew exists, correcting the late skew by selecting a second input ~~(the late skew input)~~ for receiving the plurality of data-bits, wherein the data-bits at the second input are at least one clock cycle earlier than the data-bits for the first input; and

if there is an early skew, correcting the early skew by selecting a third input ~~(the early skew input)~~ for receiving the plurality of data-bits such that the data-bits at the third input are at least one clock cycle later than the data-bits at the first input.

Claim 2. (original) The method of claim 1 wherein the communication system is a synchronous optical network (SONET).

Claim 3. (original) The method of claim 1 wherein the first chip is a system chip for performing protocol conversion and the second chip is a framer for framing and de-framing Internet protocol packets.

Claim 4. (original) The method of claim 1 further comprising searching data on the data-bus in order to detect the training sequence.

Claim 5. (original) The method of claim 1 wherein the data-bits at the second input are at least one clock cycle later than data-bits on the data-bus.

Claim 6. (original) The method of claim 1 wherein the data-bus is a 16 bit data-bus.

Claim 7. (original) A method for de-skewing data in a communication system having a system chip for transmitting a plurality of data-bits via a data-bus to a framer chip, the method comprising:

receiving a sequence of training bits at the framer;

determining whether a data skew exists by comparing the sequence of training bits received to a known sequence of training bits; and

selecting any one of three inputs to receive the plurality of data-bits, wherein a first input is selected if there is no data skew, a second input is selected if there is a late skew, or a third input is selected if an early skew occurs.

Claim 8. (original) The method of claim 7 wherein the data-bits at the second input are at least one clock cycle earlier than the data-bits for the first input.

Claim 9. (original) The method of claim 7 wherein the data-bits at the third input are at least one clock cycle later than the data-bits at the first input.

Claim 10. (original) The method of claim 7 wherein the data-bits at the second input are at least one clock cycle later than data-bits on the data-bus.

Claim 11. (original) The method of claim 7 wherein the data skew has a maximum skew of +/-1 clock cycle.

Claim 12. (canceled)

Claim 13. (currently amended) ~~The circuitry of claim 12 wherein the data select port comprises first and second select lines, and wherein the circuitry further comprises~~

A circuitry for de-skewing bit arrival times on a data-bus, the circuitry comprising:

multiplexing logic circuitry having a single data output port, a data select port, and first, second and third data input ports;

a first register, having a data input port for coupling to the data-bus and a data output port for coupling to the first data input port of the multiplexing logic circuitry;

a second register having a data input port for coupling to the data output port of the first register, and having a data output port for coupling to the second data input port of the multiplexing logic circuitry;

a third register having a data input port for coupling to the data output port of the second register, and a data output port for coupling to the third data input port of the multiplexing logic circuitry, the multiplexing logic circuitry receiving first, second and third data input signals from the data output ports of the first, second and third registers, respectively, and selectively forwarding any one of the first, second and third data input signals to its single data output port; and

control logic circuitry having first and second data output ports coupled to the first and second data select lines respectively of the multiplexing logic circuitry such that the control logic circuitry selects the first data input signal if there is a late skew, or selects the second data input signal if there is no data skew, or selects the third data input signal if an early skew occurs.

Claim 14. (original) A multiplexor logic circuitry for de-skewing data on a data-bus, the multiplexor comprising:

memory; and

logic circuitry, for receiving a first data input signal from a first register, and for receiving a second data input signal from a second register, and for receiving a third data input signal from a third register, said multiplexor selecting the first data input signal if there is a late skew at the data-bus, or selecting the second data input signal if there is no data skew, or selecting the third data input signal if an early skew occurs.

Claim 15. (original) The circuitry of claim 14 further comprising

a first register having a data input port coupled to the data-bus and having a data output port for providing the first data signal;

a second register having a data input port coupled to the data output port of the first register, and having a data output port for providing the second data signal; and

a third register having a data input port coupled to the data output port of the second register and having a data output port for providing the third data signal.

Claim 16. (original) The circuitry of claim 15 further comprising

a fourth register having a data input port communicably coupled to the data output port of the third register, and having an data output port coupled to a data input port of a fifth register.

Claim 17. (original) The method of claim 16 wherein the data on the data-bus skew has a maximum skew of +/-2 clock cycle.

Claim 18. (original) The method of claim 14 wherein the data on the data-bus skew has a maximum skew of +/-1 clock cycle.

Claim 19. (original) The method of claim 14 further comprising

searching the data on the data-bus in order to detect the training sequence.